



ALPHA DATA

FMC-CAMERALINK User Manual

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1 Introduction

The FMC-CAMERALINK is a VITA 57.1 compliant Single Width LPC FMC module, designed for use with Alpha Data's VITA 57.1 compliant carrier cards. It provides the user with the connectivity to implement computationally intensive applications such as frame grabbers, digital video communications and image processing systems in FPGA fabric.

The adapter provides the connection between the FPGA card and the industry standard **CameraLink** high-speed digital camera interface using the standard **Shrunk Delta Ribbon Connectors** from 3M.

The FMC-CAMERALINK provides support for 2 **Base** configuration inputs or one **Medium** or **Full** configuration input. In addition to being able to be used for image capture, the FMC-CAMERALINK may also be used for emulation of either up to two Base format cameras or one Medium / Full format camera.

The FMC also provides four LEDs for use as status indicators, a RS232 buffer, and two UFL connectors as additional features.

Power Over Camera Link (PoCL) is also supported by the FMC-CAMERALINK when order with the /PoCL build option.

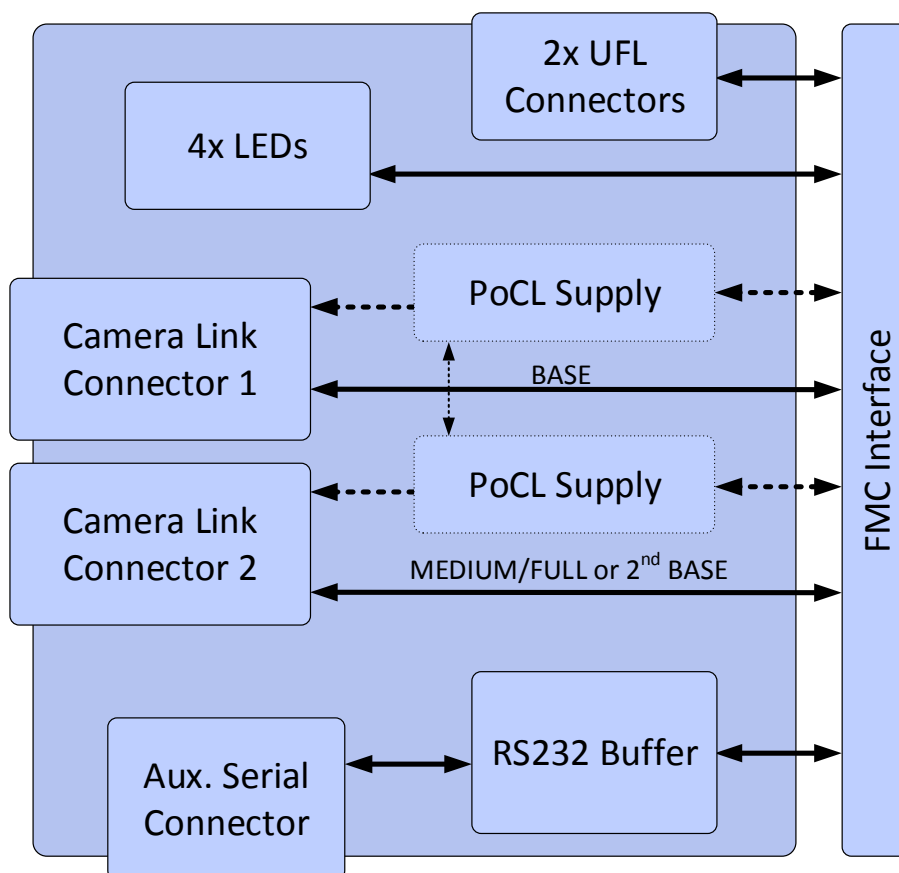


Figure 1 : FMC-CAMERALINK Block Diagram

1.1 References

Camera Link Specification v1.1 (Automated Imaging Association).

ANSI/VITA 57.1, FPGA Mezzanine Card (FMC) Standard, 2010, ISBN 1-885731-49-3

2 Specification

2.1 IO Voltage

The FMC-CAMERALINK requires the host board to provide VADJ in the range 1.8V to 3.3V.

2.2 Connectors

Camera Link: SDR connector 3M; part number 12226-8250-00FR

Auxiliary Serial: 0.1"/2.54mm pitch 3 pin right angle header.

2.3 Mating Cable-form

SDR cable assembly 3M part number 1SF26-L120-00C-XXX,

where XXX= length in centimetres.

SDR to MDR cable assembly 3M part number 1MF26-L560-00C-XXX, where XXX= length in centimetres.

Auxiliary Serial: 0.1"/2.54mm pitch female plug.

2.4 Features

Feature of the FMC-CAMERALINK are shown below.

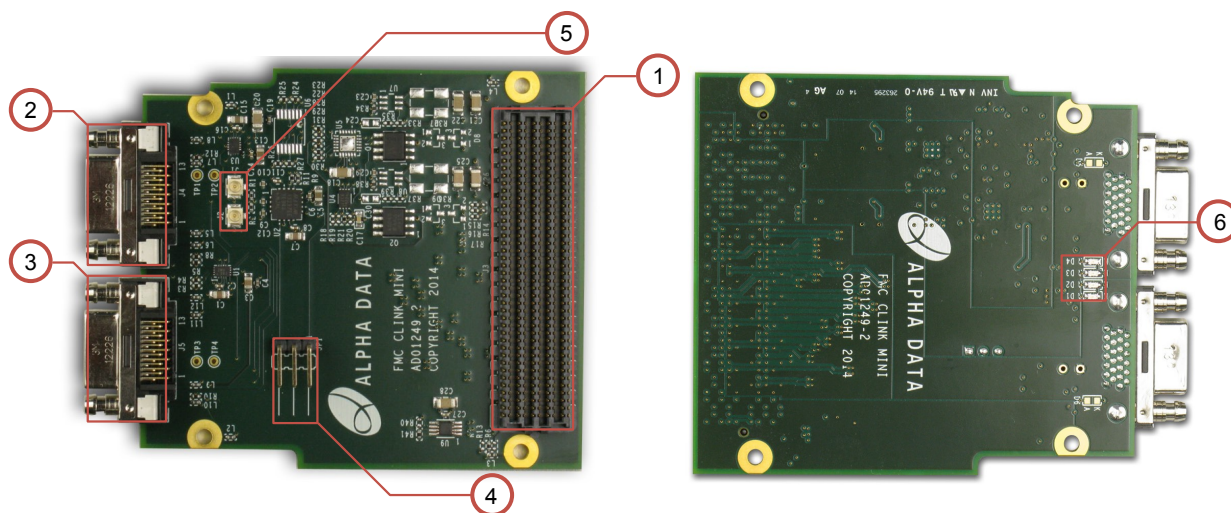


Figure 2 : FMC-CAMERALINK

Feature	Description	Feature	Description
1	FMC Connector	4	RS232 Header
2	Camera Link Connector 1	5	UFL connectors
3	Camera Link Connector 2	6	LEDs

Table 1 : FMC-CAMERALINK board features

3 Installation

The FMC-CAMERALINK is designed to plug in to the FMC front panel connector on a compatible carrier. The retaining screws should be tightened to secure the FMC.

Note: This operation should not be performed while the host PMC, XMC or PCI(e) card is powered up.

3.1 Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions.

Avoid flexing the board.

3.2 IO Voltage Selection

The host board is required to provide FMC_VADJ in the range 1.8V to 3.3V, with 1.8V preferred. This requirement is stored in a ROM on the FMC, as per VITA 57.1 for automatic configuration of supplies.

For host boards that require 1.5V operating levels (such as AMD Versal product portfolio), a custom product code is required. Please use FMC-CAMERALINK/C1 when ordering boards with 1.5V support. PoCL and The auxiliary serial connection (RS232) are not support in this build configuration.

3.3 Camera Link Full Input Configuration

When using the FMC module in a Camera Link Full Input configuration a differential termination should be instantiated across the unused LVDS pair LA_16_N/P. This can be achieved either by instantiating a terminating differential input on the attached FPGA IO pins if required, or having an external 100Ω termination located at the Camera on this unused differential pair.

4 Order Code

4.1 FMC-CAMERALINK

The FMC does not support providing power over the Camera Link Connection.

4.2 FMC-CAMERALINK/PoCL

Power can be provided by the FMC-CAMERALINK over the Camera Link connection(s) to attached camera(s).

5 Pin-out

5.1 Camera Link Pin-out

Note:

In some configurations FMC pin have the N/P pairs swapped (signals marked with '*' in the tables below). These signals will need re-inverting in the connected FPGA design.

5.1.1 Dual Base Input Configuration

The following tables show the pin usage for attaching two Base cameras to an FPGA design.

Signal Name	Direction	FMC pin	SDR pin (Con. 1)
xclk_p	in	LA_P_00	9
xclk_n	in	LA_N_00	22
x_p<0>	in	LA_P_02	12
x_n<0>	in	LA_N_02	25
x_p<1>	in	LA_P_03	11
x_n<1>	in	LA_N_03	24
x_p<2>	in	LA_P_04	10
x_n<2>	in	LA_N_04	23
x_p<3>	in	LA_P_05	8
x_n<3>	in	LA_N_05	21
cc_p<1>	out	LA_P_18	5
cc_n<1>	out	LA_N_18	18
cc_p<2>	out	LA_P_19	17
cc_n<2>	out	LA_N_19	4
cc_p<3>	out	LA_P_20	3
cc_n<3>	out	LA_N_20	16
cc_p<4>	out	LA_P_21	15
cc_n<4>	out	LA_N_21	2
ser_tfg_p	in	LA_P_14	6
ser_tfg_n	in	LA_N_14	19
ser_tc_p	out	LA_P_15	20
ser_tc_n	out	LA_N_15	7

Table 2 : Camera Link Connector 1 (Dual Base Input Configuration)

Signal Name	Direction	FMC pin	SDR pin (Con. 2)
xclk_p	in	LA_P_01	9
xclk_n	in	LA_N_01	22
x_p<0>	in	LA_P_06	12
x_n<0>	in	LA_N_06	25
x_p<1>	in	LA_P_07	11
x_n<1>	in	LA_N_07	24
x_p<2>	in	LA_P_08	10
x_n<2>	in	LA_N_08	23
x_p<3>	in	LA_P_09	8
x_n<3>	in	LA_N_09	21
cc_p<1>	out	LA_P_11	5
cc_n<1>	out	LA_N_11	18
cc_p<2>	out	LA_N_12*	17
cc_n<2>	out	LA_P_12*	4
cc_p<3>	out	LA_P_17	3
cc_n<3>	out	LA_N_17	16
cc_p<4>	out	LA_N_13*	15
cc_n<4>	out	LA_P_13*	2
ser_tfg_p	in	LA_P_10	6
ser_tfg_n	in	LA_N_10	19
ser_tc_p	out	LA_P_16	20
ser_tc_n	out	LA_N_16	7

Table 3 : Camera Link Connector 2 (Dual Base Input Configuration)

5.1.2 Base/Medium/Full Input Configuration

The following tables show the pin usage for attaching one Base/Medium or Full camera to an FPGA design.

Signal Name	Direction	FMC pin	SDR pin (Con. 1)
xclk_p	in	LA_P_00	9
xclk_n	in	LA_N_00	22
x_p<0>	in	LA_P_02	12
x_n<0>	in	LA_N_02	25
x_p<1>	in	LA_P_03	11
x_n<1>	in	LA_N_03	24
x_p<2>	in	LA_P_04	10
x_n<2>	in	LA_N_04	23
x_p<3>	in	LA_P_05	8
x_n<3>	in	LA_N_05	21
cc_p<1>	out	LA_P_18	5
cc_n<1>	out	LA_N_18	18
cc_p<2>	out	LA_P_19	17
cc_n<2>	out	LA_N_19	4
cc_p<3>	out	LA_P_20	3
cc_n<3>	out	LA_N_20	16
cc_p<4>	out	LA_P_21	15
cc_n<4>	out	LA_N_21	2
ser_tfg_p	in	LA_P_14	6
ser_tfg_n	in	LA_N_14	19
ser_tc_p	out	LA_P_15	20
ser_tc_n	out	LA_N_15	7

Table 4 : Camera Link Connector 1 (Base/Medium/Full Input Configuration)

Signal Name	Direction	FMC pin	SDR pin (Con. 2)
yclk_p	in	LA_P_01	9
yclk_n	in	LA_N_01	22
y_p<0>	in	LA_P_06	12
y_n<0>	in	LA_N_06	25
y_p<1>	in	LA_P_07	11
y_n<1>	in	LA_N_07	24
y_p<2>	in	LA_P_08	10
y_n<2>	in	LA_N_08	23
y_p<3>	in	LA_P_09	8
y_n<3>	in	LA_N_09	21
zclk_p	in	LA_P_17	3
zclk_n	in	LA_N_17	16
z_p<0>	in	LA_P_10	6
z_n<0>	in	LA_N_10	19
z_p<1>	in	LA_P_11	5
z_n<1>	in	LA_N_11	18
z_p<2>	in	LA_P_12	4
z_n<2>	in	LA_N_12	17
z_p<3>	in	LA_P_13	2
z_n<3>	in	LA_N_13	15

Table 5 : Camera Link Connector 2 (Base/Medium/Full Input Configuration)

5.1.3 Dual Base Output Configuration

The following tables show the pin usage for emulating two Base cameras from an FPGA design.

Signal Name	Direction	FMC pin	SDR pin (Con. 1)
xclk_p	out	LA_N_18*	18
xclk_n	out	LA_P_18*	5
x_p<0>	out	LA_P_21	15
x_n<0>	out	LA_N_21	2
x_p<1>	out	LA_N_20*	16
x_n<1>	out	LA_P_20*	3
x_p<2>	out	LA_P_19	17
x_n<2>	out	LA_N_19	4
x_p<3>	out	LA_N_14*	19
x_n<3>	out	LA_P_14*	6
cc_p<1>	in	LA_N_00*	22
cc_n<1>	in	LA_P_00*	9
cc_p<2>	in	LA_P_04	10
cc_n<2>	in	LA_N_04	23
cc_p<3>	in	LA_N_03*	24
cc_n<3>	in	LA_P_03*	11
cc_p<4>	in	LA_P_02	12
cc_n<4>	in	LA_N_02	25
ser_tfg_p	out	LA_N_05*	21
ser_tfg_n	out	LA_P_05*	8
ser_tc_p	in	LA_N_15*	7
ser_tc_n	in	LA_P_15*	20

Table 6 : Camera Link Connector 1 (Dual Base Output Configuration)

Signal Name	Direction	FMC pin	SDR pin (Con. 2)
xclk_p	out	LA_N_11*	18
xclk_n	out	LA_P_11*	5
x_p<0>	out	LA_N_13*	15
x_n<0>	out	LA_P_13*	2
x_p<1>	out	LA_N_17*	16
x_n<1>	out	LA_P_17*	3
x_p<2>	out	LA_N_12*	17
x_n<2>	out	LA_P_12*	4
x_p<3>	out	LA_N_10*	19
x_n<3>	out	LA_P_10*	6
cc_p<1>	out	LA_N_01*	22
cc_n<1>	out	LA_P_01*	9
cc_p<2>	out	LA_P_08	10
cc_n<2>	out	LA_N_08	23
cc_p<3>	out	LA_N_07*	24
cc_n<3>	out	LA_P_07*	11
cc_p<4>	out	LA_N_06	12
cc_n<4>	out	LA_P_06	25
ser_tfg_p	in	LA_N_09*	21
ser_tfg_n	in	LA_P_09*	8
ser_tc_p	out	LA_N_16*	7
ser_tc_n	out	LA_P_16*	20

Table 7 : Camera Link Connector 2 (Dual Base Output Configuration)

5.1.4 Base/Medium/Full Output Configuration

The following tables show the pin usage for emulating a Base/Medium or Full camera from an FPGA design.

Signal Name	Direction	FMC pin	SDR pin (Con. 1)
xclk_p	out	LA_N_18*	18
xclk_n	out	LA_P_18*	5
x_p<0>	out	LA_P_21	15
x_n<0>	out	LA_N_21	2
x_p<1>	out	LA_N_20*	16
x_n<1>	out	LA_P_20*	3
x_p<2>	out	LA_P_19	17
x_n<2>	out	LA_N_19	4
x_p<3>	out	LA_N_14*	19
x_n<3>	out	LA_P_14*	6
cc_p<1>	in	LA_N_00*	22
cc_n<1>	in	LA_P_00*	9
cc_p<2>	in	LA_P_04	10
cc_n<2>	in	LA_N_04	23
cc_p<3>	in	LA_N_03*	24
cc_n<3>	in	LA_P_03*	11
cc_p<4>	in	LA_P_02	12
cc_n<4>	in	LA_N_02	25
ser_tfg_p	out	LA_N_05*	21
ser_tfg_n	out	LA_P_05*	8
ser_tc_p	in	LA_N_15*	7
ser_tc_n	in	LA_P_15*	20

Table 8 : Camera Link Connector 1 (Base/Medium/Full Output Configuration)

Signal Name	Direction	FMC pin	SDR pin (Con. 2)
yclk_p	out	LA_N_11*	18
yclk_n	out	LA_P_11*	5
y_p<0>	out	LA_N_13*	15
y_n<0>	out	LA_P_13*	2
y_p<1>	out	LA_N_17*	16
y_n<1>	out	LA_P_17*	3
y_p<2>	out	LA_N_12*	17
y_n<2>	out	LA_P_12*	4
y_p<3>	out	LA_N_10*	19
y_n<3>	out	LA_P_10*	6
zclk_p	out	LA_N_07*	24
zclk_n	out	LA_P_07*	11
z_p<0>	out	LA_N_09*	21
z_n<0>	out	LA_P_09*	8
z_p<1>	out	LA_N_01*	22
z_n<1>	out	LA_P_01*	9
z_p<2>	out	LA_N_08*	23
z_n<2>	out	LA_P_08*	10
z_p<3>	out	LA_N_06*	25
z_n<3>	out	LA_P_06*	12

Table 9 : Camera Link Connector 2 (Base/Medium/Full Output Configuration)

5.2 Additional Features Pin-out

5.2.1 UFL connectors

The FMC-CAMERALINK provides four LEDs that can be controlled by an attached FPGA design.

Signal Name	Direction	FMC pin	Notes
led<0>	out	LA_P_25	Drive high to illuminate
led<1>	out	LA_P_26	Drive high to illuminate
led<2>	out	LA_P_27	Drive high to illuminate
led<3>	out	LA_P_28	Drive high to illuminate

Table 10 : LED Indicators

5.2.2 UFL connectors

The UFL connectors on the FMC provide direct **un-buffered** signals to the attached FPGA. These are intended for connecting high speed timing signals to the FPGA, or to be used for synchronising between FPGA boards where multiple FMC-CAMERALINKs are used.

Signal Name	Direction	FMC pin	Notes
J1	inout	LA_N_32	Un-buffered general purpose IO.
J2	inout	LA_N_33	Un-buffered general purpose IO.

Table 11 : UFLs

5.2.3 Auxiliary Serial

In addition to serial over Camera Link, a RS232 serial connection can also be connected to an attached FPGA via a RS232 buffer. The external RS232 signals should be within the ranges specified in the tables in [RX input](#) and [TX output](#)

Signal Name	Direction	FMC pin	Notes
tx	out	LA_P_29	UART output
rx	in	LA_P_30	UART input
force	out	LA_P_32	Active high enable for RS232 interface
ready	in	LA_P_31	Active high, signalling RS232 transceiver is operational.
invalid_l	in	LA_P_33	Legacy. Has behaviour matching 'ready'.

Table 12 : RS232 Interface

Signal Name	Direction	JP1 pin	Notes
txmon	out	1	RS232 compatible output
gnd		2	Ground
rxmon	in	3	RS232 compatible input

Table 13 : RS232 External

6 PoCL

This section applies only to boards build with the /PoCL order code. Board built without the /PoCL order code are not fitted with the PoCL power supplies, and current limiter circuitry.

Signal Name	Direction	FMC pin	Notes
pocl_en_a_l	out	LA_P_22	Drive low to enable PoCL to CLink Connector 1. Tri-state or drive high to clear fault or disable power.
pocl_en_b_l	out	LA_P_23	Drive low to enable PoCL to CLink Connector 2. Tri-state or drive high to clear fault or disable power.
pocl_fault_a_l	in	LA_N_22	Logic level 0 indicates a PoCL fault for Connector 1 when pocl_en_a_l is enabled.
pocl_fault_b_l	in	LA_N_23	Logic level 0 indicates a PoCL fault for Connector 2 when pocl_en_b_l is enabled.

Table 14 : PoCL Control and Status pin-out

6.1 Current limit

The FMC-CAMERALINK limits each Camera Link connector to providing up to 400mA. When the current limit is reached the supply will be disabled until the corresponding pocl_en_[a/b]_l signal is driven high.

6.2 Notes

For -full Camera Link PoCL (using both Camera Link connectors to provide power to the Camera) pocl_en_a_l and pocl_en_b_l should be driven together.

7 RS232 Electrical Specifications

The tables below show the electrical characteristics of the RS232 connection (JP1) under typical operating conditions.

RX Inputs	Min	Typ	Max	Units
Input Voltage Range	-25		25	V
Input Threshold Low	0.6	1.2		V
Input Threshold High		1.5	2.4	V
Input Hysteresis		0.5		V
Input Resistance	3	5	7	kΩ

Table 15 : RX input

TX Outputs	Min	Typ	Max	Units
Output Voltage Swing	±5	n/a	±5.4	V
Output Resistance	300	n/a	10M	Ω
Output Short-Circuit Current	n/a	n/a	±60	mA
Output Leakage Current	n/a	n/a	±60	mA

Table 16 : TX output

Revision History

Date	Revision	Nature of Change
25th Mar. 2014	2.0	Initial Release
26th Mar. 2014	2.1	Removed un-needed configuration section referencing SW1 on the Rev. 1 PCB.
18th Apr. 2014	2.2	Added documentation for /PoCL Builds
29 June 2015	2.3	Clarified PoCL and auxiliary serial functionality.
13th Mar. 2017	2.4	Correct polarity of LA_N_06/LA_P_06 in Camera Link Connector 2 (Base/Medium/Full Output Configuration) table.
1st June 2017	2.5	Example designs removed as no longer available
22nd Nov. 2018	2.6	Corrections to Camera Link Connector 2 (Base/Medium/Full Output Configuration) table.
5th Feb. 2019	2.7	Correct note (*) on inversion of LA_N_06/LA_P_06 in Camera Link Connector 2 (Base/Medium/Full Output Configuration) table.
8th Jan. 2026	2.8	Added C1 order option to IO Voltage Selection .